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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,862	09/30/2003	Chao-Yuan Su	TSM03-0150	1880

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EXAMINER	
TOLEDO, FERNANDO L	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 11/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,862	SU ET AL.	
	Examiner	Art Unit	
	Fernando L. Toledo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-64* is/are pending in the application.

4a) Of the above claim(s) *47-64* is/are withdrawn from consideration.

5)☒ Claim(s) *33-46* is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hara et al. (U. S. Patent 5,371,411 A) in view of Yasuda et al. (U. S. Patent 6,876,946 B2).

3. In re claim 1, Hara, in the U. S. Patent 5,371,411 A; figures 1 – 13D does not disclose a first scribe line having a selected width extending along a first direction and adjacent a first die of the multiplicity of dies a second scribe line having a selected width extending along a second direction adjacent the first die and intersecting the first scribe line at a corner point of the first die; at least one free area defined on at least one of the first and second scribe lines where placement of a test key is restricted.

However, Yasuda, in the U. S. Patent 6,876,946 B2; figures 1 – 23 and related text, discloses a first scribe line having a selected width extending along a first direction and adjacent a first die of the multiplicity of dies a second scribe line having a selected width extending along a second direction adjacent the first die and intersecting the first scribe line at a corner point of the first die (Figure 3 and Figure 6); at least one free area defined on at least one of the first and second scribe lines where placement of a test key is restricted (Figure 14B) to provide an alignment method of aligning each of processing areas on the wafer with a predetermined

position at high speed and with accuracy even though the processing areas on the wafer are expanded, contracted or rotated (Column 4, Lines 57 – 62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the scribe lines of Yasuda in the invention of Hara, since as taught by Yasuda, it provides an alignment method of aligning each of processing areas on the wafer with a predetermined position at high speed and with accuracy even though the processing areas on the wafer are expanded, contracted or rotated.

4. In re claim 2, Hara discloses wherein at least one layer of the wafer structure is a low-k dielectric layer (Column 4, Lines 27 – 31).

5. In re claim 3, Hara discloses wherein the low-k dielectric layer has a dielectric constant of less than approximately 3.5 (Column 4, Lines 27 – 31).

6. In re claim 4, Hara discloses wherein the low-k dielectric layer has a dielectric constant of less than 3.0 (Column 4, Lines 27 – 31).

7. In re claim 5, Hara discloses wherein the low-k dielectric layer is a material selected from the group consisting of CVD, SiOC, SiOCN, SiOC, CVD polymer, spin-on polymer, FSG, SiO_2 and combinations thereof (Column 4, Lines 27 – 31).

8. In re claim 6, Hara discloses wherein the free area is a free are A_1 on the first scribe line and is defined by the equation $A_1=D_1 \text{ X } S_1$ where D_1 is the distance along the first direction extending from the corner point of the die, and S_1 is the width of the first scribe line (Figures 13A – 13D).

9. In re claim 7, Hara discloses wherein the free area is defined on the top of the multi-layer structure (Figure 4).

10. In re claim 8, Hara discloses wherein the free area is defined on at least one of the top three layers of the multi-layer structure (Figures 4 and 9).

11. In re claim 9, Hara discloses at least one test key formed in the free area, the at least one test key having a measurement ration R_1, wherein the measurement ratio is defined by the equation $R_1=M_1/A_1$, wherein M_1 is the total area of the at least one test key formed on the free area A_1 and R_1 is less than about 10% (Figures 13A – 13D).

12. In re claim 10, Hara discloses wherein the distance D_1 is less than about 600 μm (Figure 13A – 13D).

13. In re claim 11, Hara discloses wherein the width S_1 of the first scribe line is greater than about 20 μm (Figure 13A – 13D).

14. In re claim 12, Hara discloses wherein the multi-layer structure is formed on a substrate selected from the group consisting of bulk Si, SOI, SiGe, GaAs, InP, and a combination thereof (Column 3, Lines 46 – 49).

15. In re claim 13, Hara discloses wherein the die includes: a first peripheral region inside on an extending parallel to the first scribe line 13; a second peripheral region inside of an extending parallel to the second scribe line 13 and intersecting the first peripheral region to form a corner area 4; a conductive ring 12 formed between the die and the first peripheral region and the second peripheral region; and an array of apertures formed in the conductive ring and adjacent the corner area of the die (Figure 4).

16. In re claim 14, Hara discloses wherein the array of apertures includes at least two slots (Figure 13A – 13D).

17. In re claim 15, Hara discloses wherein the array of apertures includes two rows of holes (Figures 13A – 13D).

18. In re claim 16, Hara discloses wherein the array of apertures extends along at least one of the first peripheral regions and the second peripheral region (Figure 13A – 13D).

19. In re claim 17, Hara discloses wherein the die further includes a circuit area with several circuit elements, wherein the conductive ring is electrically connected to the circuit elements to apply one of a power source and a ground potential to the circuit elements (Figure 4).

20. In re claim 18, Hara discloses wherein the conductive ring has a width of between 50 μm and about 300 μm (Figure 11).

21. In re claim 19, Hara discloses wherein the free area is a free area A_s at the intersection of the first scribe line and the second scribe line and is defined by the equation $A_s = S_1 \text{ X } S_2$, wherein S_1 is the width of the first scribe line and $S_2$is the width of the second scribe line (Figure 13A – 13B).

22. In re claim 20, Hara discloses further including at least one test key formed on the free area A_s, the test key having a measurement ratio R_s that is less than 10% and is defined by the equation $R_s = M_s / A_s$, wherein M_s is the total area of the at least one test key formed on the free area A_s (Figure 13A – 13B).

23. In re claim 21, Hara discloses wherein the width of the scribe line S_1 and S_2 is greater than about 20 μm (Figure 13A – 13D).

24. In re claim 22, Hara discloses wherein the at least one free area includes a first free area A_1 on the first scribe line and a second free area A_2 on the second scribe line, the first free area defined by the equation $A_1 = D_1 \text{ X } S_1$ where D_1 is the distance along the first direction extending

from the corner point of the die and S_1 is the width of the first scribe line, the second free area defined by the equation $A_2 = D_2 \text{ X } S_2$ where D_2 is the distance along the second direction extending from the corner of the point of the die and S_2 is the width of the second scribe line (Figure 13A – 13D).

25. In re claim 23, Hara discloses including a third free area A_s at the intersection of the first scribe line and the second scribe line is defined by the equation $A_s = S_1 \text{ X } S_2$ (Figure 13A – 13D).

26. In re claim 24, Hara discloses at least one test key formed on at least one of the free areas A_1, A_2 and A_s; wherein a first measurement ratio R_1 is defined as the equation $R_1 = M_1 / A_1$, wherein M_1 is the total area of the test keys formed on the first free area A_1; wherein the second measurement ratio R_2 is defined as the equation $R_2 = M_2 / A_2$, wherein M_2 is the total area of the test keys formed on the second free area A_2; wherein the third measurement ratio R_s is defined as the equation $R_s = M_s / A_s$, wherein M_s is the total area of the test keys formed on the second free area A_s; and wherein the total measurement ratio R is defined as the equation $R = (M_1+M_2+ M_s) / (A_1+A_2+A_s)$ (Figures 13A – 13D).

27. In re claim 25, Hara discloses wherein R_1 is less than about 10% (Figures 13A – 13D).

28. In re claim 26, Hara discloses wherein R_2 is less than about 10% (Figure 13A – 13D).

29. In re claim 27, Hara discloses wherein R_s is less than about 10% (Figure 13A – 13D).

30. In re claim 28, Hara discloses wherein the R is less than about 10% (Figure 13A – 13D).

31. In re claim 29, Hara discloses wherein the first distance D_1 is less than about 600 μm (Figures 13A – 13D).

32. In re claim 30, Hara discloses wherein the second distance D_2 is less than about 600 μm (Figures 13A – 13D).

33. In re claim 31, Hara discloses wherein the width S_1 of the first scribe is greater than about 20 μm (Figures 13A – 13D).

34. In re claim 32, Hara discloses wherein the width S_2 of the second scribe line is greater than about 20 μm (Figures 13A – 13D).

Allowable Subject Matter

35. Claims 33 – 46 are allowed over the prior art of record.

Response to Arguments

36. Applicant's arguments with respect to claims 1 – 46 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando L. Toledo whose telephone number is 571-272-1867. The examiner can normally be reached on Mon-Thu 7am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fernando L. Toledo
Patent Examiner
Art Unit 2823

flt
7 November 2005